Syllabus

Course Number: CS 440
Course Title: Computer Organization and Architecture

Course Description

CS 440 - COMPUTER ORGANIZATION AND ARCHITECTURE (3). Introduces Machine Architecture with coverage of digital logic, machine level data and instruction representation, ALU design, and organization of the processor datapath and control. Examines performance analysis, memory system hierarchy, pipelining, and communication.

Prerequisite Courses

CS390 Principles of Programming Languages
AND
CS324 Algorithms & Complexity

(or CS370 Assembly Language -- only for degree plans prior to Fall 2015)

Please note that CS210/CS310 are pre-requisites to CS390 and CS324 (and CS361/CS362 are pre-requisites to CS370), so knowledge of the subjects covered in those courses will also be assumed. You need to have a working knowledge of the following topics within each course:

1. Practice with problem definition, solution construction, top-down design techniques, algorithmic development, documentation, testing, debugging, and maintenance (CS361/CS362 or CS210/CS310).

2. Ability to use control structures including: if and switch statements and while, do-while, and for loops (CS361 or CS210) and data structures (CS362 or CS310).

Course Overview

The computer lies at the heart of computing. All students of computing should acquire some understanding and appreciation of a computer system's functional components, their characteristics, their performance, and their interactions.

It is important to understand Computer Architecture in order to structure a program so that it runs efficiently on a real machine. And when selecting a system to use, it is important to understand the tradeoff among various components, so you can accurately compare competing systems, and understand technical literature on new computer systems.
This course will cover the basic concepts of Computer Architecture that are important for you to understand, including the CPU control and datapath, memory systems including caching and virtual memory, and input/output subsystems.

**WARNING to students:**

Many students find *this course* to be one of the *more difficult* of the courses in the Regis Computer Science curriculum. So please be sure you will have adequate time to devote to this course before taking it.

**Course Outcomes**

Upon completion of this course, students should be able to:

1. Explain digital logic and its use in digital systems.
   a. Describe the progression of computer architecture from vacuum tubes to VLSI.
   b. Detail the basic building blocks and their role in the historical development of computer architecture.
   c. Use mathematical expressions to describe the functions of simple combinational and sequential circuits.
   d. Design a simple circuit using the fundamental building blocks.

2. Understand machine level representation of data.
   a. Explain the reasons for using different formats to represent numerical data.
   b. Explain how negative integers are stored in sign-magnitude and twos-complement representation.
   c. Explain how floating point numbers are stored in IEEE formats.
   d. Convert numerical data from one format to another.
   e. Discuss how fixed-length number representations affect accuracy and precision.
   f. Perform simple mathematical and logical operations upon numerical data.
   g. Describe the internal representation of nonnumeric data.

3. Understand assembly level machine organization.
   a. Explain the organization and functional units of the classical von Neumann machine, and explain how instructions are executed on it.
   b. Summarize how instructions are represented, at both the machine and assembly levels, for a specific instruction set design.
   c. Explain how instruction formats vary, such as addresses per instruction and variable length vs. fixed length formats.
   d. Write simple assembly language program segments.
   e. Demonstrate how fundamental high-level programming constructs are implemented at the machine-language level.

4. Describe the functional organization of a processor datapath and performance enhancements.
   a. Explain a single cycle datapath implementation.
   b. Compare alternative implementations of datapaths (e.g. multicycle).
   c. Discuss the concept of control points and the generation of control signals.
d. Explain basic instruction level parallelism using pipelining and the major hazards that may occur.
e. Describe the implementation of hazard detection and use of register-forwarding for data hazard reduction.
f. Explain the concept of branch prediction and how it is used.
g. Characterize the costs and benefits of prefetching.
h. Explain speculative execution and identify the conditions that justify it.

5. Describe memory system organization and architecture.
   a. Identify the main types of memory technology.
   b. Explain the effect of memory latency on running time and how the memory hierarchy reduces the effective memory latency.
   c. Describe the principles of memory management.
   d. Describe the role of cache and compare and contrast direct, fully-associative and set-associative cache organizations.
   e. Explain the workings of a system with virtual memory management.

6. Describe interfacing and communication.
   a. Explain how interrupts are used to implement I/O control and data transfers.
   b. Identify various types of buses in a computer system.
   c. Describe data access from a magnetic disk drive and flash drive.

7. Understand technical literature on computer systems.

8. Analyze a computer system's expected performance.
   a. Analyze how each component of a computer system affects performance.
   b. Measure performance using benchmarks and performance metrics.

Course Materials

Required Text:

Technology Tools:

PowerPoint Viewer (online):
Some of the course content is presented via PowerPoint slide shows. If needed, you can download the free PowerPoint viewer via this link:

Course Policies and Procedures

Adding this course during the Drop/Add Period
If you added this course during the drop/add period, after class began on Monday, you are responsible for *immediately* notifying the instructor that you joined the course late. None of the course due dates will be extended for you. Even if a due date already passed when you added the course, late points will still be deducted.

**Repeating the course**

If you are repeating this course (due to a previous withdraw or low grade), you are responsible for *immediately* notifying the instructor. Course assignments that you submitted when you last took the course cannot be repeated -- you will be required to complete alternate assignments.

**Academic Integrity**

Plagiarism includes submitting work obtained from any person, publication, or internet web source. All work submitted in CS440 must be your own.

In cases of suspected cheating or plagiarism, the instructor will discuss the matter with the student(s) involved. The instructor reserves the right to question any student orally or in writing about any assignment, and to use the evaluation of the student's understanding of the assignment and of the submitted solution as evidence of cheating.

All cheating and plagiarism incidents will be reported to the Academic Integrity Board.
**Pre-Assignment**

Read the week 1 reading assignments in your textbook. Be *prepared* to *ask questions* on unclear areas and *to respond* to questions.

**Online Format:** Sign on to worldclass.regis.edu and become familiar with the course navigation of the Web Curriculum. Complete assignments above.

**Classroom-based Format:** Complete assignments above by the first night of class.
## Course Assignments and Activities

<table>
<thead>
<tr>
<th>Week</th>
<th>Topics</th>
<th>Readings*</th>
<th>Activities Assignments and Associated Points**</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>• Computer Systems and Current Technology</td>
<td>Ch. 1: Sec 1.1 – 1.5</td>
<td>Participation in Discussions 12% for entire course</td>
</tr>
<tr>
<td></td>
<td>• Numbering Systems and Numeric Representations</td>
<td>Ch. 2: Sec 2.1 – 2.4</td>
<td></td>
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<tr>
<td></td>
<td>• Arithmetic and Logic Operations and Units</td>
<td>Ch. 3: Sec 3.1 – 3.3, page 196 to top of 211 of Sec 3.5</td>
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<td></td>
<td></td>
<td>Appendix B: Sec B.1 – B.3</td>
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<tr>
<td>2</td>
<td>• Arithmetic and Logic Operations and Units (cont)</td>
<td>Ch. 2: Sec 2.5 – 2.7, 2.10 – 2.12, and 2.19 – 2.20, 2.10 – 2.18</td>
<td>Participation in Discussions</td>
</tr>
<tr>
<td></td>
<td>• Instruction Set Architecture</td>
<td>Optional: Sec 2.16 – 2.18</td>
<td>Exam #1 16%</td>
</tr>
<tr>
<td>3</td>
<td>• Instruction Processing and the Datapath (single cycle)</td>
<td>Appendix B Sec B.5 pages B-26 – B-35, Sec B.7 all, and Sec B.8, pages B-50 – B-56</td>
<td>Participation in Discussions / Project Overview</td>
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<tr>
<td></td>
<td>• Performance Analysis</td>
<td>Ch 1, Sec 1.6</td>
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<td>Ch 4: Sec 4.1 – 4.4</td>
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<tr>
<td>4</td>
<td>• Instruction Processing and the Datapath (multi-cycle)</td>
<td>Appendix B Sec B.5 pages B-26 – B-35, Sec B.7 all, and Sec B.8, pages B-50 – B-56</td>
<td>Participation in Discussions</td>
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<tr>
<td></td>
<td>• Performance Analysis</td>
<td>Ch 1, Sec 1.6</td>
<td>Exam #2 16%</td>
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<td>Ch 4: Sec 4.1 – 4.4</td>
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<tr>
<td>5</td>
<td>• Pipelining</td>
<td>Ch 4: Sec 4.5 – 4.8, 4.13 – 4.14</td>
<td>Participation in Discussions</td>
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<td>Optional: Sec 4.11</td>
<td>Project Draft</td>
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<tr>
<td>6</td>
<td>• Memory Hierarchy</td>
<td>Appendix B: Sec B.9</td>
<td>Participation in Discussions</td>
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<tr>
<td></td>
<td></td>
<td>Ch 5: Sec 5.1 – 5.8 and 5.15 – 5.16</td>
<td>Exam #3 16%</td>
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<tr>
<td>7</td>
<td>• Input and Output (I/O)</td>
<td>Ch 5: Sec 5.11</td>
<td>Participation in Discussions</td>
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<tr>
<td>8</td>
<td>None</td>
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<td>Final Project 24%</td>
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<td>Final Exam 16%</td>
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<td><strong>Note to Classroom sections only:</strong> Your instructor's syllabus, handed out the first night of class, will indicate any changes to this grid. Classroom requirements for the Final Project and Presentations will be handed out in class.</td>
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*Previous Edition Reading Assignments:* Alternate reading assignments for the previous edition of the textbook (4th edition) will be available in your instructor's syllabus.

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Exams
There will be four exams. The first 3 exams will be online, timed exams, and the last exam will be an essay exam. Exam questions will be cumulative, taken from reading assignments and course content.

Final Project
Each student will submit a final project, covering the details of one specific architecture.

Participation
Participation is important because we can all learn from each other. Your participation points can make a difference in the final grade. Participation means:
   1. a. Present in class every session (classroom)
      b. Present in the discussion forum every week (online)
   2. a. Effectively responds to questions from the facilitator (classroom)
      b. Checks discussion forum and posts required items by the deadlines (online)
   3. Interacts/replies to other students in classroom/forum discussions.

Summary of Assignments and Percentage Weight towards course grade

<table>
<thead>
<tr>
<th>Assignment</th>
<th>Value (percent of overall course grade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Participation</td>
<td>12%</td>
</tr>
<tr>
<td>Exams (4 exams at 16% each)</td>
<td>64%</td>
</tr>
<tr>
<td>Final Project</td>
<td>24%</td>
</tr>
<tr>
<td>Totals</td>
<td>100%</td>
</tr>
</tbody>
</table>

See your instructor’s faculty syllabus in WorldClass for the online Discussion points distribution.

CC&IS Policies and Procedures
Each term, students are expected to review the CC&IS Policies and Procedures Syllabus Addendum, located at [http://idt.regis.edu/syllabi/syllabus_addendum.html](http://idt.regis.edu/syllabi/syllabus_addendum.html), which covers:

- CC&IS Grading Scale
- Academic Honor Code and Integrity Policy
- Student Standards of Conduct
- Human Subjects Institutional Review Board (IRB)

The CC&IS Policies & Procedures Syllabus Addendum also summarizes additional important policies including, Diversity, Equal Access, Disability Services, and Attendance & Participation, etc that apply to every course offered by the College of Computer & Information Sciences at Regis University.