REGIS UNIVERSITY

COLLEGE OF COMPUTER & INFORMATION SCIENCES

Syllabus

Course Number: CS 440
Course Title: Computer Organization and Architecture

Course Description:

CS 440 - COMPUTER ORGANIZATION AND ARCHITECTURE (3). Introduces machine architecture through the traditional Von Neumann architectural schemes. Features traditional register-to-register transfer logic, ALU design, and BUS architectures. Examines hamming codes, disk drive performance analysis, virtual storage and cache memory, pipelining, micro-code and bit-slicing. Examines several systolic architectures and their corresponding parallel processing environments.

Prerequisite Courses:

CS449 Algorithms & Complexity
or
CS370 Assembly Language (degree plans prior to Fall 2015)
or
CS435 (traditional Regis College students only)

Please note that CS202/CS210/CS310 are pre-requisites to CS449 and CS208/CS361/CS362 are pre-requisites to CS370, so knowledge of the subjects covered in those courses will also be assumed. You need to have a working knowledge of the following topics within each course:

1. Knowledge of basic CPU components and data representation in binary (*CS208 or CS202*).

2. Understanding of the Fetch-Decode-Execute instruction cycle and how basic Assembly Language commands execute (*CS208 or CS202*).

3. Practice with problem definition, solution construction, top-down design techniques, algorithmic development, documentation, testing, debugging, and maintenance (*CS361/CS362 or CS210/CS310*).

4. Ability to use control structures including: if and switch statements and while, do-while, and for loops (*CS361 or CS210*) and data structures (*CS362 or CS310*).

5. Understanding of modular code design with functions, procedures, and proper parameter passing, using both pass-by-value and pass-by-reference (*CS362 or CS310*).

Course Overview

The computer lies at the heart of computing. All students of computing should acquire some understanding and appreciation of a computer system's functional components, their characteristics, their performance, and their interactions.

It is important to understand Computer Architecture in order to structure a program so that it runs efficiently on a real machine. And when selecting a system to use, it is important to understand the tradeoff among various components, so you can accurately compare competing systems, and understand technical literature on new computer systems.

This course will cover the basic concepts of Computer Architecture that are important for you to understand, including the CPU control and datapath, memory systems including caching and virtual memory, and input/output subsystems.

WARNING to students:

Many students find ***this course*** to be one of the ***more difficult*** of the courses in the Regis Computer Science curriculum. Be sure you will have adequate time to devote to this course before taking it!

Course Outcomes:

Upon completion of this course, learners should be able to:

1. Explain digital logic and its use in digital systems.
   a. Describe the progression of computer architecture from vacuum tubes to VLSI.
   b. Detail the basic building blocks and their role in the historical development of computer architecture.
   c. Use mathematical expressions to describe the functions of simple combinational and sequential circuits.
   d. Design a simple circuit using the fundamental building blocks.

2. Understand machine level representation of data.
   a. Explain the reasons for using different formats to represent numerical data.
   b. Explain how negative integers are stored in sign-magnitude and twos-complement representation.
   c. Explain how floating point numbers are stored in IEEE formats.
   d. Convert numerical data from one format to another.
   e. Discuss how fixed-length number representations affect accuracy and precision.
   f. Perform simple mathematical and logical operations upon numerical data.
   g. Describe the internal representation of nonnumeric data.

3. Understand assembly level machine organization.
   a. Explain the organization and functional units of the classical von Neumann machine, and explain how instructions are executed on it.
   b. Summarize how instructions are represented, at both the machine and assembly levels, for a specific instruction set design.

c. Explain how instruction formats vary, such as addresses per instruction and variable length vs. fixed length formats.
d. Write simple assembly language program segments.
e. Demonstrate how fundamental high-level programming constructs are implemented at the machine-language level.

4. Describe the functional organization of a processor datapath and performance enhancements.
   a. Explain a single cycle datapath implementation.
   b. Compare alternative implementations of datapaths (e.g. multicycle).
   c. Discuss the concept of control points and the generation of control signals.
   d. Explain basic instruction level parallelism using pipelining and the major hazards that may occur.
   e. Describe the implementation of hazard detection and use of register-forwarding for data hazard reduction
   f. Explain the concept of branch prediction and how it is used.
   g. Characterize the costs and benefits of prefetching.
   h. Explain speculative execution and identify the conditions that justify it.

5. Describe memory system organization and architecture.
   a. Identify the main types of memory technology.
   b. Explain the effect of memory latency on running time and how the memory hierarchy reduces the effective memory latency.
   c. Describe the principles of memory management.
   d. Describe the role of cache and compare and contrast direct, fully-associative and set-associative cache organizations.
   e. Explain the workings of a system with virtual memory management.

6. Describe interfacing and communication.
   a. Explain how interrupts are used to implement I/O control and data transfers.
   b. Identify various types of buses in a computer system.
   c. Describe data access from a magnetic disk drive.
   d. Describe the advantages and limitations of RAID architectures.

7. Understand technical literature on computer systems.

8. Analyze a computer system's expected performance.
   a. Analyze how each component of a computer system affects performance.
   b. Measure performance using benchmarks and performance metrics.

Course Materials:

Required Texts:

Patterson, David A., Hennessy, John L., (2014), *Computer Organization and Design: the Hardware /Software Interface,* (5th Edition). Morgan Kaufmann Publishers, ISBN-13: 978-0124077263, ISBN-10: 0124077269.

Technology Tools:

PowerPoint Viewer (online):

Some of the course content is presented via PowerPoint slide shows. If needed, you can download the free PowerPoint viewer via this link:

http://www.microsoft.com/en-us/download/details.aspx?id=13

Pre-Assignment:

Read the week 1 reading assignments in your textbook.
Be ***prepared*** to ***ask questions*** on unclear areas and ***to respond*** to questions.

Online Format: Sign on to worldclass.regis.edu and become familiar with the course navigation of the Web Curriculum. Complete assignments above.

Classroom-based Format: Complete assignments above by the first night of class.

Course Assignments and Activities:

	Topics	Readings*	Activities Assignments and Associated Points**
1	• Computer Systems and Current Technology • Numbering Systems and Numeric Representations • Arithmetic and Logic Operations and Units	Ch. 1: Sec 1.1 – 1.5 Ch. 2: Sec 2.1 – 2.4 Ch. 3: Sec 3.1 – 3.3, page 196 to top of 211 of Sec 3.5 Appendix B: Sec B.1 – B.3	Participation in Discussions 11% for entire course
2	• Arithmetic and Logic Operations and Units (continued) • Instruction Set Architecture	Ch. 2: Sec 2.5 – 2.7, 2.10 – 2.12, and 2.19 – 2.20 Optional: Sec 2.16 – 2.18	Participation in Discussions Exam #1 16%
3	• Instruction Processing and the Datapath (single cycle) • Performance Analysis	Appendix B Sec B.5 pages B-26 – B-35, Sec B.7 all, and Sec B.8, pages B-50 – B-56 Ch 1, Sec 1.6 Ch 4: Sec 4.1 – 4.4	Participation in Discussions
4	• Instruction Processing and the Datapath (multi-cycle) • Performance Analysis	Appendix B Sec B.5 pages B-26 – B-35, Sec B.7 all, and Sec B.8, pages B-50 – B-56 Ch 1, Sec 1.6 Ch 4: Sec 4.1 – 4.4	Participation in Discussions Exam #2 16%
5	• Pipelining	Ch 4: Sec 4.5 – 4.8, 4.13 – 4.14 Optional: Sec 4.11	Participation in Discussions
6	• Memory Hierarchy	Appendix B: Sec B.9 Ch 5: Sec 5.1 – 5.8 and 5.15 – 5.16	Participation in Discussions Exam #3 16%
7	• Input and Output (I/O)	Ch 5: 5.11	Participation in Discussions Final Project 25%
8		None	Participation in Discussions Final Exam 16%
		Total	**100%**

****Previous Edition Reading Assignments:*** Alternate reading assignments for the previous edition of the textbook (4th edition) will be available in your facilitator's syllabus.

*****Note to Classroom sections only:*** Your facilitator's syllabus, handed out the first night of class, will indicate any changes to this grid. Classroom requirements for the Final Project and Presentations will be handed out in class.

Summary of Assignments and Percentage Weight towards course grade

Assignment	Value (percent of overall course grade)
Participation	**11%**
Exams (4 exams at 16% each)	**64%**
Final Project	**25%**
Totals	100 %

Exams
There will be 4 exams. Exam questions will be cumulative, taken from reading assignments and course content.

Final Project
Each student will submit a final project, covering the details of one specific architecture.

Course Policies and Procedures

Adding this course during the Drop/Add Period

If you added this course during the drop/add period, after class began on Monday, you are responsible for ***immediately*** notifying the instructor that you joined the course late. None of the course due dates will be extended for you. Even if a due date already passed when you added the course, late points will still be deducted.

Repeating the course

If you are repeating this course (due to a previous withdraw or low grade), you are responsible for ***immediately*** notifying the instructor. Course assignments that you submitted when you last took the course cannot be repeated -- you will be required to complete alternate assignments.

CC&IS Grading Scale

Letter Grade	Percentage	Grade Point
A	93 to 100	4.00
A–	90 to less than 93	3.67
B+	87 to less than 90	3.33
B	83 to less than 87	3.00
B–	80 to less than 83	2.67
C+	77 to less than 80	2.33
C	73 to less than 77	2.00
C–	70 to less than 73	1.67
D+	67 to less than 70	1.33
D	63 to less than 67	1.00
D-	60 to less than 63	.67
F	Less than 60	0

Additional information about grading can be found in the latest edition of the University Catalog, available at http://www.regis.edu/Academics/Course%20Catalog.aspx.

CC&IS Policies and Procedures

Each of the following CC&IS Policies & Procedures is incorporated here by reference. Students are expected to review this information each term, and agree to the policies and procedures as identified here and specified in the latest edition of the University Catalog, available at http://www.regis.edu/Academics/Course%20Catalog.aspx or at the link provided.

- The CC&IS Academic Integrity Policy.
- The Student Honor Code and Student Standards of Conduct.
- Incomplete Grade Policy, Pass / No Pass Grades, Grade Reports.
- The Information Privacy policy and FERPA. For more information regarding FERPA, visit the U.S. Department of Education.
- The HIPPA policies for protected health information. The complete Regis University HIPAA Privacy & Security policy can be found here: http://www.regis.edu/About-Regis-University/University-Offices-and-Services/Auxiliary-Business/HIPAA.aspx.
- The Human Subjects Institutional Review Board (IRB) procedures. More information about the IRB and its processes can be found here: http://regis.edu/Academics/Academic-Grants/Proposals/Regis-Information/IRB.aspx.

The CC&IS Policies & Procedures Syllabus Addendum summarizes additional important policies including, Diversity, Equal Access, Disability Services, and Attendance & Participation that apply to every course offered by the College of Computer & Information Sciences at Regis University.

A copy of the CC&IS Policies & Procedures Syllabus Addendum can be found here: https://in2.regis.edu/sites/ccis/policies/Repository/CCIS%20Syllabus%20Addendum.docx.